A study on EMI noise source modeling with voltage source in synchronous DC-DC buck converter

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***Abstract*—This paper studies electromagnetic interference noise source modeling with voltage source for electromagnetic compatibility design of synchronous DC-DC buck converter. The transient response of switching node voltage contains surge and ringing oscillation which can be attained by solving differential equation of power loop equivalent circuit model in the tested converter.**

Keywords—synchronous DC-DC buck converter, equivalent circuit model, ringing oscillation, inverse Laplace transform

I. INTRODUCTION

There is an increasing demand for high efficiency and high power density of power converters. Fast switching operation of power semiconductor devices will reduce the switching loss. High-frequency switching leads to high power density due to reduced size and weight of passive components. However, the switching operation with high *dv/dt* and *di/dt* may induce surge and ringing oscillation by interacting with circuit parasitic components, that results in generating electromagnetic interference (EMI) noise. Particularly in the development of electric vehicles, EMC requirement is strictly regulated because EMI can occur failure of other devices and leads to critical accidents. Estimating and mitigating EMI noise of power supply in the early design phase helps to reduce both cost and time of R&D. Many approaches have been studied to predict EMI noise [1]-[4]. Behavioral modeling (black box modeling) method doesn't require the detail design information of the circuit and can obtain relatively accurate results [5][6]. However, it is difficult to apply this method to early phase of circuit design, because it requires a lot of measurement of input and output responses for target. In addition, behavioral modeling is limited in frequency domain analysis. Physics-based model, like equivalent circuit model, can estimate time domain response, though it requires detail characteristics of circuit components. This report proposes the equivalent circuit model of the power loop in the tested synchronous DC-DC buck converter composed of CMOS transistor, which is commonly applied to power supply for ECU (Electrical Control Unit) in a vehicle. This article especially focuses on the transient response of switching node voltage (V_{SW}) to evaluate EMI noise source of the tested power supply with solving differential equation of the equivalent circuit model.

II. EQUIVALENT CIRCUIT MODELING OF POWER LOOP

Fig. 1 shows the circuit diagram and circuit operating condition of tested synchronous rectification DC-DC buck converter. High *di/dt* is induced on the power loop composed of input capacitor C_{in} and MOSFETs, Q_H, Q_L shown in Fig. 1, for turn-on and turn-off operation. Fig. 2 depicts the waveform of switching node voltage (V_{SW}) in one switching cycle.

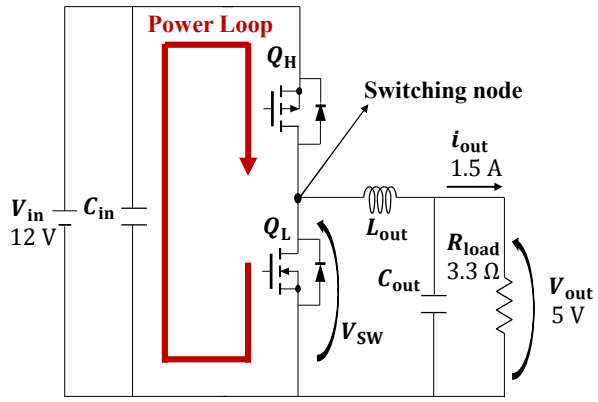

Fig. 1. Synchronous DC-DC buck converter
($f_{sw} = 1.42\ MHz$)

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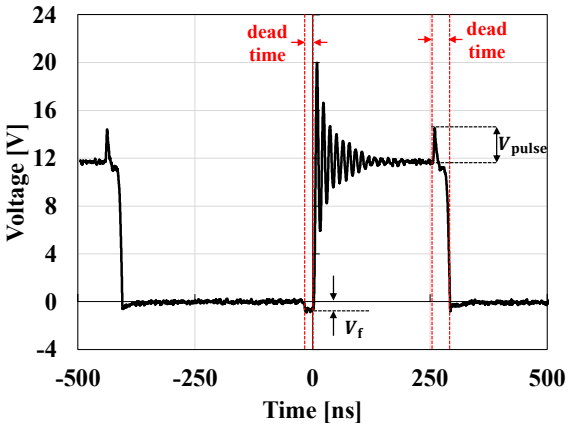

Fig. 2. Measured switching node voltage V_{SW} contains surge and ringing oscillation

V_{sw} contains forward voltage drop of body diode (V_f) and surge voltage due to *di/dt* in high side turn-off operation (V_{pulse}). Distinct surge and ringing oscillation appear in V_{sw} waveform, especially in Q_L turn-off operation as shown in Fig. 2. This section explains the evaluation results of the parasitic components in the power loop to model this transient response.

A. *Input smoothing capacitor*

Passive components in the tested circuit are smoothing input capacitor (C_{in}), smoothing output inductor (L_{out}), smoothing output capacitor (C_{out}) and load resistance (R_{load}). Parasitic components of the input smoothing capacitor (C_{in}) could affect noise characteristics. The applied C_{in} is two parallel connected surface mount type (1210 size) of multi-layer ceramic capacitor (MLCC) (GRM32ER71E226ME, murata). The ESL and ESR of the C_{in} are identified by 2-port shunt-through measurement [7] with vector network analyzer (E5061B, Keysight) (VNA). Shunt-through measurement enable high accuracy measurement of low impedance. The applied C_{in} (with applying 12V DC bias) can be modeled RLC series circuit identified as $R = 1.9\ m\Omega, L = 0.17\ nH, C = 18.6\ \mu F$.

B. *PCB trace*

The parasitic inductance of the PCB trace dominates power loop inductance. Equivalent circuit model of PCB trace identified from the frequency characteristics of impedance, which are measured with impedance analyzer (E4990A, Keysight) and 2-port vector network analyzer (E5061B, Keysight). It is also calculated by EM analysis (Advanced Design System, Keysight) based on method of moment. PCB design of tested board and the port for measurement and calculation is shown in Fig. 3. Each separated lands in the power loop except for C_{in} terminal are short-connected for the evaluation of the trace impedance. Fig. 4 shows the measured and calculated frequency characteristic of PCB trace impedance from C_{in} terminal (w/o C_{in}). In addition, Fig. 5 shows the measured and calculated frequency characteristics of power loop inductances.

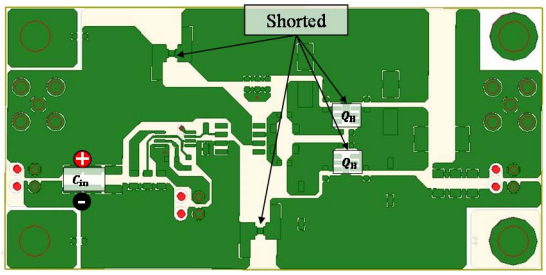

Fig. 3. PCB design of tested circuit and port in measurement and calculation

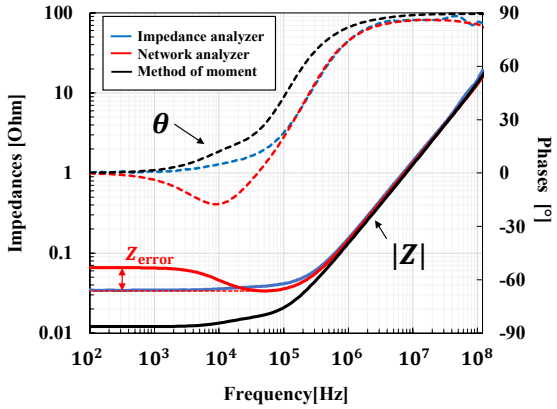

Fig. 4. Measured ant calculated power loop impedances and phase of PCB trace

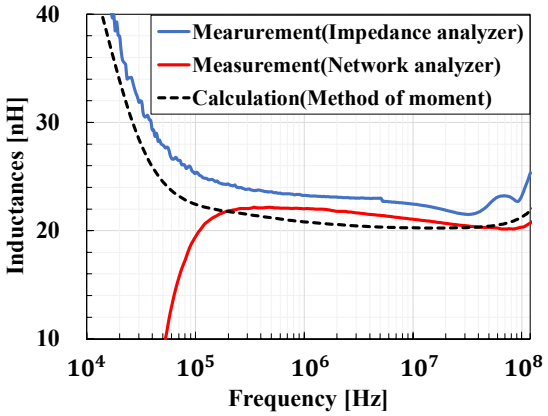

Fig. 5. Measured and calculated power loop inductances of PCB trace

The measured characteristics of inductive reactance well agree with the EM calculation result. The calculation result of 21.4 nH is applied to equivalent circuit model in this study. The difference (Z_{error}) between two measurement results are stemming from the cable shield resistance (braided wire resistance) at low-frequency (~300 kHz) in shunt-through measurement [8]. The two measured minimum impedance in low frequency (~10 kHz) agree well, which corresponds to power loop resistance of PCB. However, calculated impedances in low frequency is too small and different from measured results, because resistance of conductor is neglected. Therefore, the measured resistance is added to equivalent circuit for PCB trace.

C. Equivalent circuit model of MOSFETs

MOSFET has three terminals and it is not appropriate to apply 1-port measurement by impedance analyzer and shunt-through measurement, because the rest floating terminal may influence on measurement result. The parasitic inductances of TSOP-6 package MOSFET is evaluated with 2-port measurement by network analyzer (E5061B, Keysight). The applied MOSFETs (BSL306N and BSL308PE) have two N(P)-channel MOSFETs in one package. They are connected in parallel for the studied circuit and used as a single MOFET. The measurement ports are connected to the MOSFET as shown in Fig. 6 (a) and (b). Two-terminal pair model is expressed by like star connected model as shown in Fig. 6 (c).

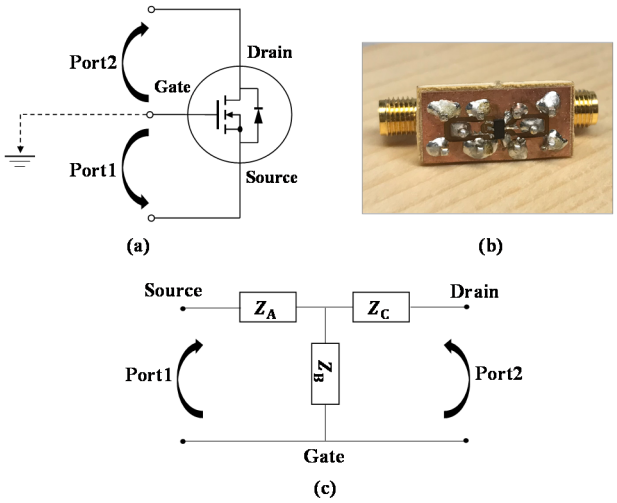

Fig. 6. (a) 2-Port connection between MOSFET and VNA (b) Test fixture for measurement and implemented MOSFET (c) Two-port network representation of MOSFET equivalent circuit

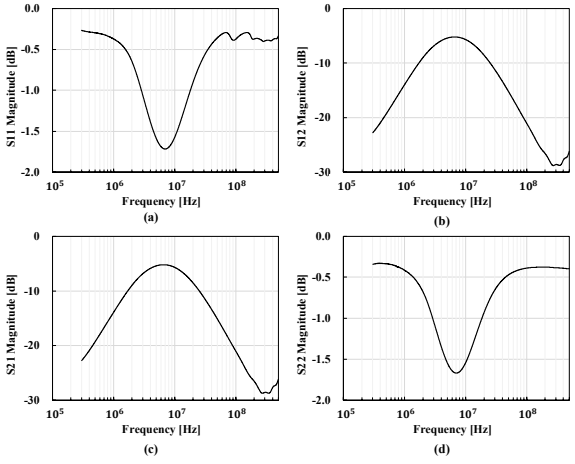

Fig. 7. Measured S-parameter of low side MOSFET. (a)S_{11}; (b)S_{12}; (c)S_{21}; (d)S_{22}

The measured 2-port S-parameter (w/o DC bias) is shown in Fig. 7. The Z parameters of star connected model shown in Fig. 6 (c) are calculated from following equations (1)-(3) with measured 2-port S parameters by VNA shown in Fig. 7 [10].

$$Z_A = 50\left[\frac{(1+S_{11})(1-S_{22})-S_{21}-S_{12}+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}}\right] \quad (1)$$

$$Z_B = 50\left[\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}}\right] \quad (2)$$

$$Z_C = 50\left[\frac{(1-S_{11})(1+S_{22})-S_{21}-S_{12}+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}}\right] \quad (3)$$

Fig. 8 shows the calculated frequency characteristics of Z_A, Z_B and Z_C. From the results of calculated impedances, Z_A, Z_B and Z_C are modeled as RLC series circuit. The parasitic inductances of MOSFET L_G, L_S and L_D in TABLE I are extracted from the resonance frequencies (f_{res}) in Z_A, Z_B and Z_C based on following equation (4), where C is the capacitances extracted from capacitive reactance of Z_A, Z_B and Z_C. The impedances at resonance frequencies of Z_A, Z_B and Z_C is equal to parasitic resistance. However, the parasitic resistances of MOSFET depend on DC bias voltage, so the calculation result of resistances are not applied.

$$L = \frac{1}{(2\pi f_{res})^2 C} \quad (4)$$

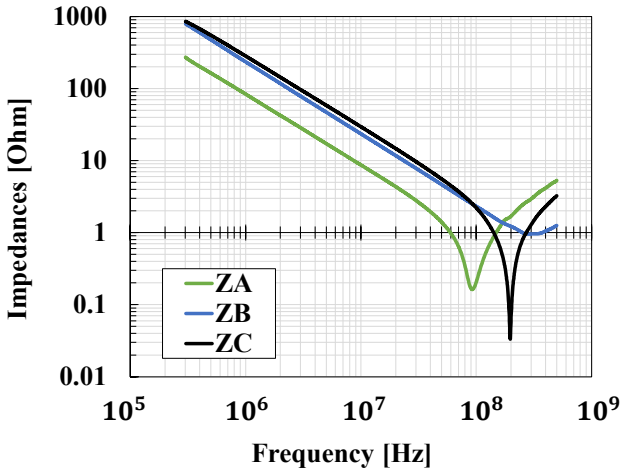

Fig. 8. Calculated Z-parameter of star-connected model

TABLE I. EXTRACTED TERMINAL INDUCTANCES

Terminal	Inductance [nH]
L_G	0.48
L_S	1.55
L_D	1.16

This study focuses on the transient response of V_{SW} for low side MOSFET turn-off operation. Therefore, high side TSOP-6 package Pch-MOSFET Q_H (BSL308PE, Infineon) is assumed as ON-state, and is modeled with series connected on resistance (R_{ON}) and a parasitic lead inductance (L_{DS}). The lead inductance (L_{DS}) is evaluated as the sum of drain inductance (L_D) and source inductance (L_S) with neglecting mutual inductance. Low side TSOP-6 package Nch-MOSFET Q_L (BSL306N, Infineon) is assumed as OFF-state, and is modeled series connected output capacitance (C_{oss}),

ESR in OFF-state (R_{oss}) [9] and parasitic lead inductance (L_{DS}). C_{oss} is measured by impedance analyzer with applying 12V DC bias voltage. The ESR of OFF-state low side MOSFET (R_{oss}) dominates the sum of resistance in power loop and greatly affects attenuation characteristics of ringing oscillation. Fig. 9 shows the measured frequency characteristics of power loop impedance with applying 12 V DC bias on C_{in} terminal (w/o C_{in}). The series resonance at 73.4 MHz is caused by total inductance in power loop (L_{loop}) and C_{oss} of Q_L. Resistance R_{oss} dominates impedance at series resonant frequency (1.36 Ω). The extracted power loop equivalent circuit model parameters are shown in Fig. 10.

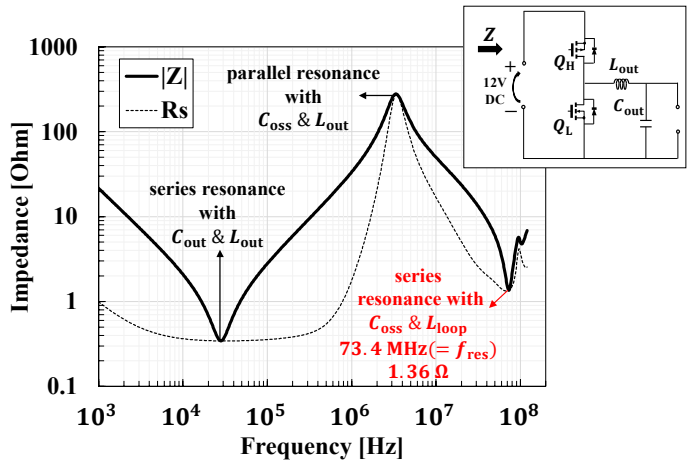

Fig. 9. Measured impedance of power loop (w/o C_{in})

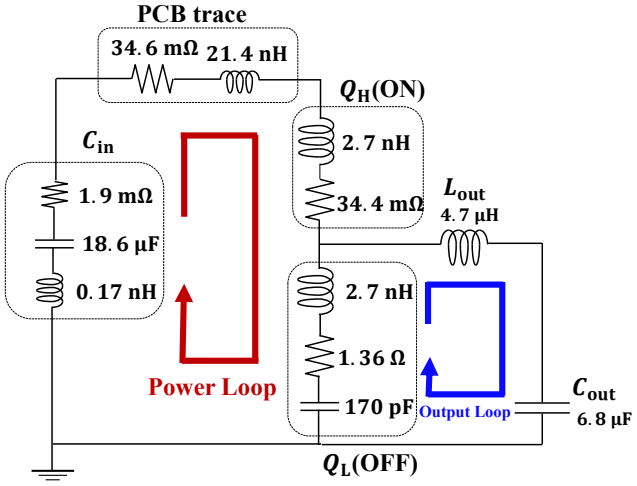

Fig. 10. Equivalent circuit model of power loop

Measured and calculated impedances of power loop from Q_L terminal (w/o Q_H) with applying 12V DC bias on Q_L terminal is shown in Fig. 11. The calculated frequency characteristics of impedance corresponds to the measured results. Therefore, the equivalent circuit model is validated.

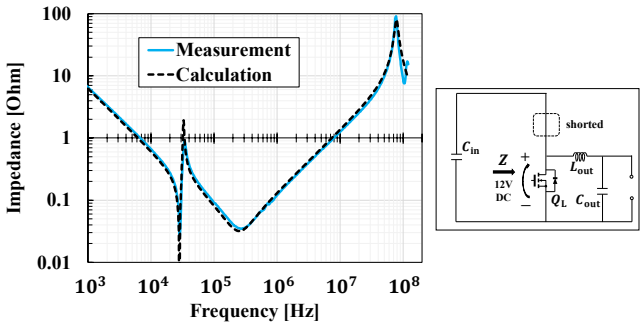

Fig. 11. Measured and calculated impedances of power loop with 12 V DC bias on Q_L terminal (w/o Q_H).

III. IDENTIFICATION OF VOLTAGE SOURCE MODEL

Ramp voltage source shown in Fig. 12 (i), equal to voltage drop for turn-off operation of Q_H, is applied as excitation noise source in series with ON-state Q_H in the equivalent circuit model of Fig. 10. The voltage source can be expressed by superposition of two ramp function shown in Fig. 12 (ii) and (iii) [11].

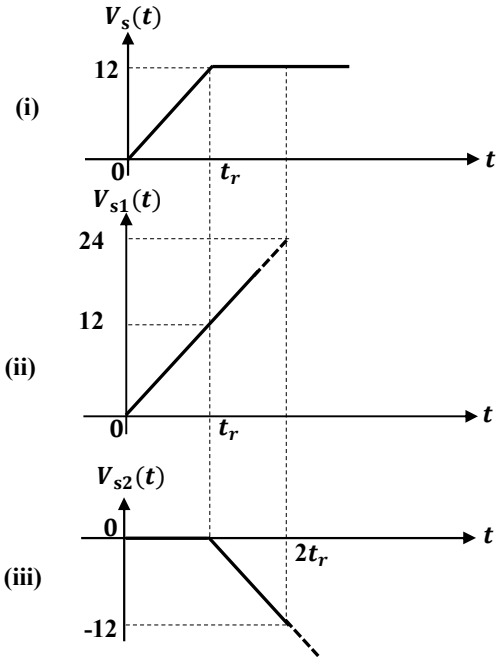

Fig. 12. (i) Ramp voltage source applied to equivalent circuit model (ii)(iii) Divided ramp voltage sources

The voltage variation shown in Fig. 12 are expressed in following equations, where t_r the rise time of $V_s(t)$.

$$V_{s1}(t) = \frac{12}{t_r} t \cdot u(t) \quad (5)$$

$$V_{s2}(t) = -\frac{12}{t_r}(t - t_r) \cdot u(t - t_r) \quad (6)$$

$$V_s(t) = V_{s1}(t) + V_{s2}(t) \quad (7)$$

Equivalent circuit model of power loop in Fig. 10 can be abbreviated to a RLC series circuit, where $R = 1.43\ \Omega, L = 27.0$ nH and $C = 170$ pF. The differential equation of RLC

series circuit can be solved algebraically by inverse Laplace transform. The differential equation of RLC series circuit when the voltage source $V_s(t)$ is applied is given by (8).

$$V_s(t) = Ri(t) - L \cdot \frac{di(t)}{dt} + \frac{1}{C}\int_0^t i(t)\,dt \qquad (8)$$

Current flowing in a RLC series circuit $i_1(t)$, $i_2(t)$ when the voltage source is $V_{s1}(t)$ and $V_{s2}(t)$ is given by following equations with applying inverse Laplace transform to (8):

$$i_1(\mathrm{t}) = \frac{12}{t_\mathrm{r}}\left\{1 - \frac{1}{\cos\theta}\mathrm{e}^{-\frac{R}{2L}t}\cos(\omega t - \theta)\right\} \qquad (9)$$

$$i_2(t) = -\frac{12}{t_r}\left[1 - \frac{1}{\cos\theta}e^{-\frac{R}{2L}(t-t_r)}\cos\{\omega(t-t_r) - \theta\}\right] \qquad (10)$$

,where $\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$, $\theta = \sin^{-1}\frac{R}{2}\sqrt{\frac{C}{L}}$.

Therefore, current flowing in a RLC series circuit *i(t)* with the voltage source is $V_s(t)$ can be written in (11).

$$i(t) = \begin{cases} i_1(t) & (0 \le t \le t_\mathrm{r}) \\ i_1(t) + i_2(t) & (t \ge t_\mathrm{r}) \end{cases} \qquad (11)$$

The rise time of voltage source (t_r) affects surge voltage (V_surge). The voltage of capacitor in the RLC series circuit $V_\mathrm{C}(t)$ is equal to the third term of (8) and can be written in (12), which almost corresponds with V_SW.

$$V_\mathrm{C}(t) = \frac{1}{C}\left[\int_0^{t_\mathrm{r}} i_1(t)\,dt + \int_{t_\mathrm{r}}^{t}\{i_1(t) + i_2(t)\}\,dt\right] \qquad (12)$$

The measured and calculated V_surge correspond when the $t_\mathrm{r} = 5$ ns. The rising part of measured and calculated V_SW and applied voltage source $V_\mathrm{s}(t)$ for $t_\mathrm{r} = 5.0$ ns are shown in Fig. 13.

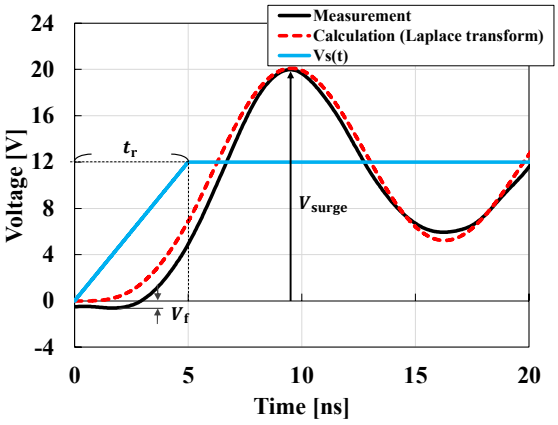

Fig. 13. The rising part of measured and calculated $\boldsymbol{V_{SW}}$ and applied voltage source $\boldsymbol{V_S(t)}$

The forward voltage V_f of body diode appears just before rising of V_SW[12]. It is difficult to consider effect of body diode characteristics because equivalent circuit model in this study is expressed as liner time-invariant RLC circuit. The calculated result shown in Fig. 13 is the voltage of C_oss in Q_L. R_oss and L_DS of Q_L is exist between probing point. Therefore, the measured V_SW is not the terminal voltage of C in lumped RLC series circuit (V_C) but the terminal voltage of equivalent circuit model of Q_L (V_SW) shown in Fig. 14. The measurement and calculation port is shown in Fig. 14. The calculated terminal voltage of equivalent circuit model of Q_L for ADS SPICE is shown in Fig. 15. The spectrum of V_SW is shown in Fig. 16.

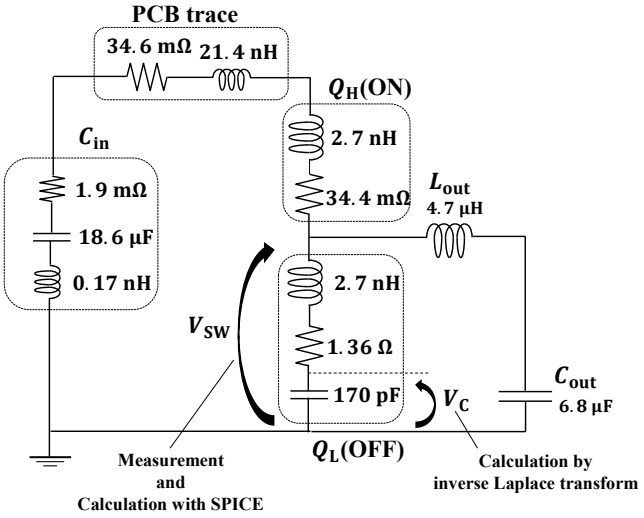

Fig. 14. Differences of Measurement and calculation port

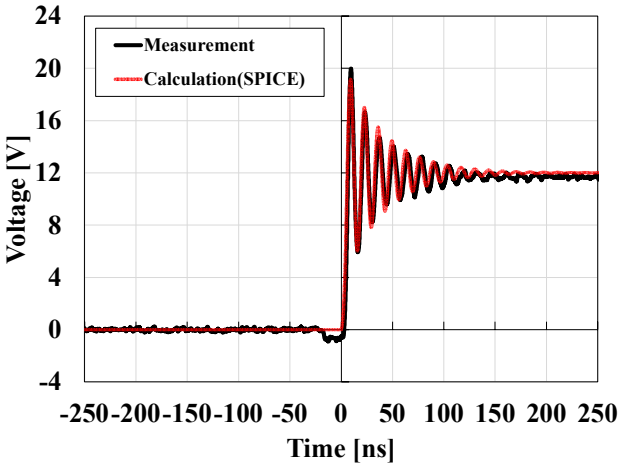

Fig. 15. The measured and calculated waveform of $\boldsymbol{V_{SW}}$

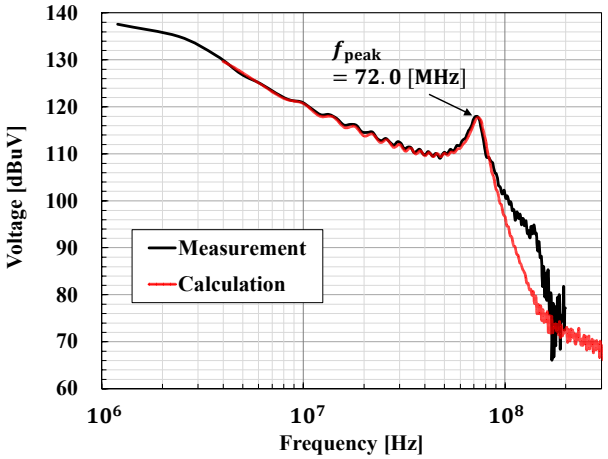

Fig. 16. The measured and calculated spectrum of V_{SW}

The calculated waveform and spectrum of V_{SW} almost corresponds with the measured result as shown in Fig. 15 and Fig. 16, respectively. The resistance which corresponds with damping characteristics of oscillation is identified as 1.39 Ω from time constant of oscillation convergence in V_{SW}. It almost corresponds to the sum of resistances in the power loop (1.43 Ω) shown in Fig. 10. The spectrum peak appears at ringing frequency (f_{peak}) in Fig. 16. f_{peak} depends on the design of PCB trace and applied components used in the circuit, and it significantly influences on the spectrum of conducted EMI. Proposed model can expect the f_{peak}. As these results, the developed model can characterize surge and ringing oscillation in the switching operation.

IV. CONCLUSION

This paper developed equivalent circuit model of parasitic components in power loop and noise source model for synchronous DC-DC buck converter. The measured and calculated waveform of switching node voltage are almost identical in both time and frequency domain, and the proposed model is validated. Further study is needed for noise source modeling to evaluate the frequency spectrum of conducted EMI for the DC-DC converter. This model will be effective to elucidate the generation mechanism of EMI noise for power supply circuit.

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